Attorney Docket No.: 42390.P4024 Patent

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

D Response 1-500

In Re Application of:

**Dalvi**

Serial No.: 08/814,928

Filed: March 12, 1997

For: STATUS INDICATORS FOR FLASH MEMORY

Art Unit: 2752

Examiner: Robertson, D.

Assistant Commissioner
for Patents
Washington, D.C. 20231

## AMENDMENT

Sir:

In response to the Office Action mailed July 23, 1999, Applicant respectfully requests the Examiner to consider the following remarks:

### REMARKS

Applicant respectfully requests reconsideration of this application.

Claims 1-11, 20-25 and 30 are pending in this application.

Claims 1-11, 20-25 and 30 are rejected under 35 U.S.C. §103(a) as being obvious in view of applicant's admitted prior art, or alternatively, U.S. Patent 5,561,628 (hereinafter referred to as Terada).

Applicants respectfully submit that claims 1-11, 20-25 and 30 are not anticipated by Terada or the alleged admitted prior art. Terada teaches an IC card including a test circuit for applying a signal potential to a plurality of control signal output terminals for placing a plurality of flash memories in a write enable state. Although the admitted prior art teaches a status register with an erase suspend status indicator (ESS), that prior art teaches away from suspending